jet INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2010, VOL. 56, NO. 4, PP. 399–404
Manuscript received October 21, 2010; revised November 2010. DOI: 10.2478/v10177-010-0053-9

Low Power, High Dynamic Range Analogue Multiplexer for Multi-Channel Parallel Recording of Neuronal Signals Using Multi-Electrode Arrays

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***Abstract*—In the paper we present the design and test results of an integrated circuit combining a sample&hold circuit and an analogue multiplexer. The circuit has been designed as a building block for a multi-channel Application Specific Integrated Circuit (ASIC) for recording signals from alive neuronal tissue using high-density micro-electrode arrays (MEAs). The design is optimised with respect to critical requirements for such applications, i.e. short sampling time, low power dissipation, good linearity and high dynamic range. Presented design comprises sample&hold circuits with class AB operational amplifier, novel shift register, which allows minimising cross-coupling of the clock signal and control logic. The circuit has been designed in $0.35\mu\mathrm{m}$ CMOS process and has been successfully implemented in a prototype multi-channel ASIC.**

***Index Terms*—Analogue multiplexer, low power amplifier, multi-channel electronics, multi-electrode arrays, neural signal.**

I. Introduction

MODERN experimental neuroscience explores widely MEAs for electrical stimulation and recording signals from neural tissue. High-density arrays comprising tens or hundreds of electrodes drive development of multi-channel integrated circuits for selective recording of neuronal signals and electrical stimulation of individual neurons [1], [2], [3]. Important building blocks of such integrated circuits are sample&hold (S&H) circuits and analogue multiplexers. A multiplexer is required to reduce the number of output data links as for a system comprising several hundreds of stimulation/recording channels it is not feasible technically and it would be expensive to transmit signals from each individual electrode to a data acquisition system via a separate cable.

A common procedure in recording from multi-electrode arrays employs continues sampling of analogue waveforms and digitisation in an external ADC [4],[1]. Given the frequency spectrum of typical neuronal signals with the upper limit not exceeding a few kHz, the required sampling rate is in a range of a few tens of kHz. Thus, the data from multiple recording channels can be digitised using a single fast ADC.

In a typical measurement sequence the signals are sampled at the same time in all the channels and then the sampled values are read out through a multiplexer and routed to single output. For example, for a 64-channel integrated circuit and sampling rate of $20\,kHz$, the multiplexing rate should be at least $1.28\,MHz$. However, a trend in neuroscience experiments is to increase the number of electrodes and so the number of readout channels. A system with 512 readout channels has been demonstrated and used successfully for performing useful measurements [1]. In such systems one can imagine multiplexing of data from larger number of chips into one ADC and then the multiplexing rate inside each chip has to be appropriately higher, e.g. $5.12\,MHz$ for four 64-channel chips or $10.24\,MHz$ for eight 64-channel chips. In the presented design we target a multiplexing rate at least $5.12\,MHz$, which for a typical sampling frequency of $20\,kHz$ will allow multiplexing 256 channels, e.g. four 64-channel chips, to one external ADC.

In contrast to stand-alone multiplexers, which are basically arrays of switches, the multiplexer in our design is essentially built into a multi-channel S&H circuit. Thus, the circuit can be considered as an analogue shift register with parallel writing and serial reading.

Previously developed multi-channel ASICs for recording neuronal signals employ a design of the analogue multiplexer controlled by the shift register with the **walking one** [5]. A drawback of such a solution is a clock feed-through appearing in the middle of the multiplexing period. After some optimisation effort the clock feed-through can be minimised, but it cannot be eliminated completely. In order to overcome this problem a novel design of the shift register has been developed. In our design the **walking one** is shifted every half of the clock period, instead of every full clock cycle.

Other critical aspect of the presented circuit is the dynamic range. Since the developed multiplexer is foreseen to be merged with the recording amplifier/filter circuits of expanded dynamic range compared to the previous designs, the dynamic range of the multiplexer has to match the dynamic range of that circuit. The requirement concerning the dynamic range is driven by the experiments employing electrical stimulation of neurons. The stimulation currents injected into the solution comprising the electrodes generate large artefacts in the recording amplifiers [6],[7]. Since the elicited spikes are superimposed on these artefacts it is important that the total signal composed of the artefact and the actual spike does not exceed the linear range of the whole recording chain.

Next very important requirement for our circuit is low power consumption. First level of limitation on the power consumption is due to experimental constraint on temperature

This work was supported by the Polish Ministry of Science and Higher Education funds in the years 2009-2012.

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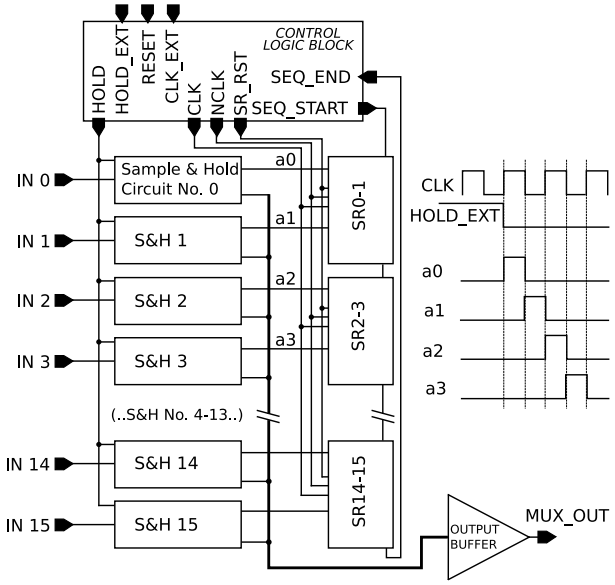

Fig. 1. Block diagram of the analogue multiplexer.

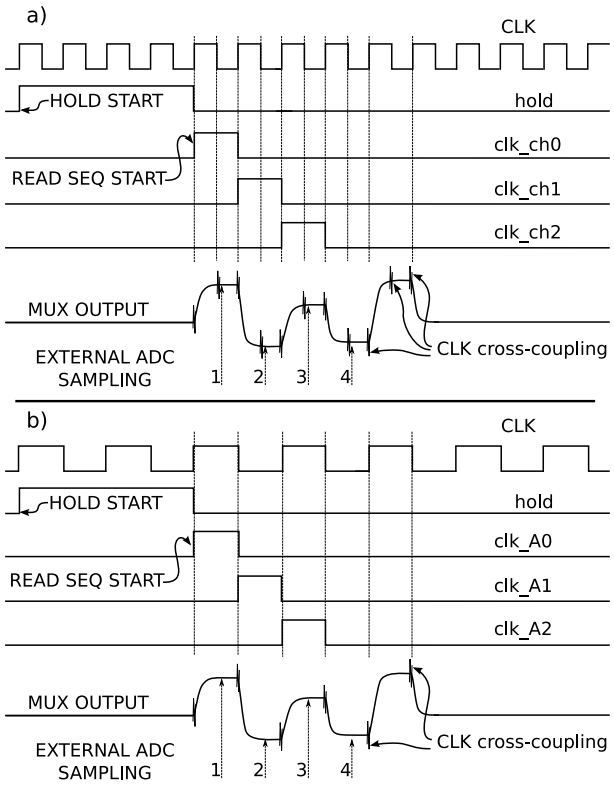

Fig. 2. a) Timing sequence of a multiplexer with a walking one shift register based on D-latches vs. b) Shift register sensitive to positive and negative clock edge.

of the integrated circuits mounted in the immediate vicinity of the array with alive neuronal tissue, which has to be kept at constant temperature. Second level of limitation is imposed by in-vivo experiments, in which the recording electronics is held by a freely moving animal, for example a rat, and has to be powered from a battery [8]. In case of a power hungry electronics the battery dominates the total weight of the set-up.

The developed 16-channel multiplexer has been integrated with the prototype 16-channel recording electronics [9]. Thus, the aspects related to the layout and possible influence of switching noise generated by the multiplexer control circuit on sensitive low noise amplifiers can be evaluated.

II. Multiplexer Design

A simplified block diagram of the analogue multiplexer is shown in Fig. 1. The circuit comprises sixteen S&H cells, eight shift register cells, and the control logic. Each cell of the shift register controls operation of two S&H cells. The control logic block is responsible for generating the sampling signal (HOLD), starting and stopping the shift register sequence and synchronization of the external control signals. Multiplexer output is buffered with a class AB amplifier, which ensures capability to drive the external capacitive load.

Several designs of multiplexers developed in the past are based on the concept of a shift register with **walking one** described in [10]. The shift register is built as a chain of serially connected D-latches triggered synchronously with the external clock. Each latch activates readout of one S&H cell. A drawback of this circuit is the clock feed-through to the output line. The glitches occur synchronously with every positive and negative clock edge. Figure 2a shows the timing diagram of such a multiplexer. Signal clk_ch0, which controls readout of the S&H cell in channel 0, is set to high level at the positive clock edge and lasts for one clock period. The next positive clock edge shifts the **one** to the neighbouring channel, signal clk_ch1 is set to high level and the signal sampled in channel #1 is transferred to the output line. The glitches on the MUX_OUTPUT caused by the positive clock edges are unavoidable. But, the negative clock edges do not trigger any operation while they generate glitches on the output line.

In order to avoid parasitic clock feed-through in the middle of the multiplexing period a novel scheme to control the readout of S&H cells has been worked out. In the new scheme the readout is controlled by a shift register that generates high output in response to the positive and to the negative clock edge. Figure 2b shows the timing diagram of the new scheme to generate the **walking one**. During one clock period the multiplexing signals for two consecutive channels are generated: clk_A0 triggered by the rising edge and clk_A1 triggered by the falling edge of the clock signal. The MUX_OUTPUT line is disturbed by the clock feed-through only when the multiplexer output is switched to the next S&H cell. Comparison of the MUX_OUTPUT waveforms in a) and b) of Fig. 2 shows clearly the advantage of the new solution.

A. Control Logic

For the present prototype the control signals are supplied externally. The control logic block generates internal control signals necessary for operation of the multiplexer in response to the three external signals: HOLD_EXT, CLK_EXT and RESET. The input analogue waveforms are sampled simultaneously at all inputs in response to the positive edge of the

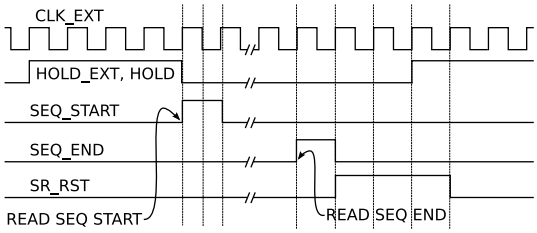

Fig. 3. Timing sequence of a control logic block. SEQ_START positive edge triggers multiplexing sequence start, after last channel readout the last activated shift register block send SEQ_END signal to control logic block.

HOLD signal. The negative edge of the HOLD signal is used to disconnect the hold capacitors from the inputs and to start multiplexing sequence by sending SEQ_START signal to the first shift register cell (SR0-1, Fig. 1). After each multiplexing sequence including all the channels the SEQ_END signal issued by the last cell of the shift register triggers the SR_RST signal which performs asynchronous reset of the shift register (see Fig. 3). Then next sequence of multiplexing starts in response to next rising edge of the HOLD signal.

B. S&H Circuit

A schematic diagram of the pair of S&H cells is shown in Fig. 4. Single cell comprises a class AB operational amplifier, six switches and a sampling capacitor C_0. In order to ensure rail-to-rail dynamic range of the sampling circuit complementary CMOS switches with local inverters have been implemented. The dimensions of PMOS and NMOS transistors in the switches are $5\,\mu m/1\,\mu m$ and $3\,\mu m/1\,\mu m$ respectively to balance the switch resistance and to minimise multiplexer non-linearity. One shift register cell controls switches of two S&H cells. Signals clk_A0, clk_B0 and clk_C0 are triggered by the positive edge of the CLK, and clk_A1, clk_B1, clk_C1 are triggered by the negative edge of the CLK, if the READ_IN signal was high during previous CLK period. The input voltage with respect to the ground potential (V_{GND}) is held on the

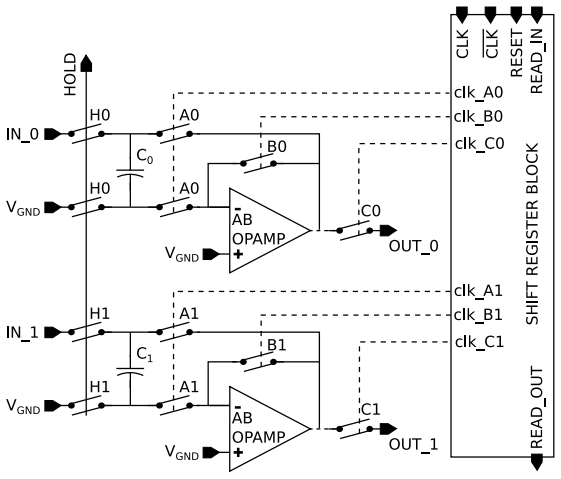

Fig. 4. A pair of S&H circuits with switches controlled by one common shift register cell.

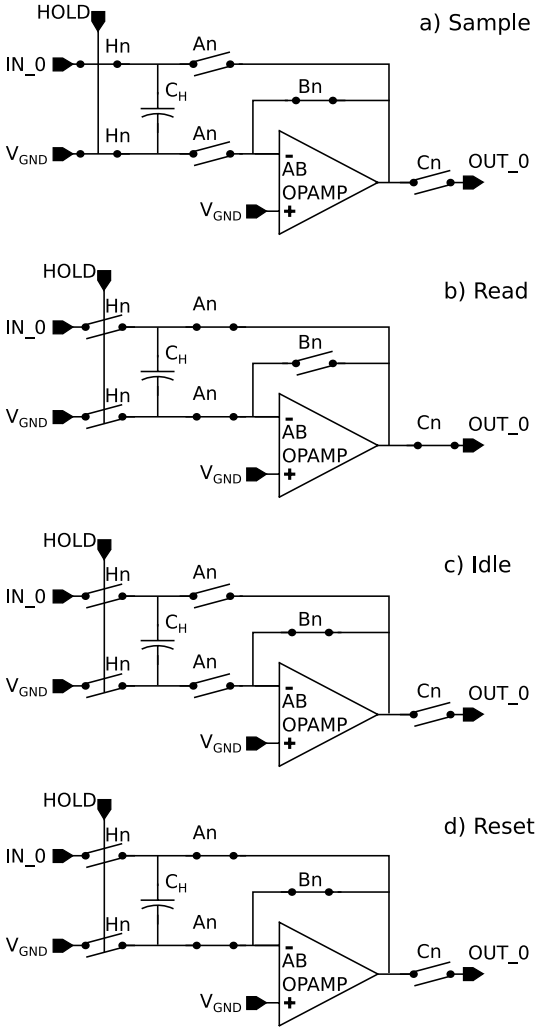

Fig. 5. Operating modes of single S&H circuit.

capacitance C_0. Outside the sampling period the hold capacitor is disconnected from the input as well as from the reference V_{GND} potential to minimise noise injection from the power supply lines.

One operation cycle of the circuit, including four phases: HOLD, READ, IDLE and RESET, is illustrated in Fig. 5.

- During the SAMPLE phase switches Hn (n corresponds to the channel number) are closed and the hold capacitor is charged to voltage $V_{IN} - V_{GND}$. Switches An, Cn are open, switch Bn is closed so that the operational amplifier works as a voltage follower.
- The READ phase is active only in one channel at the time and lasts for a half of the CLK period. Switches Hn are open, An and Cn are closed, so that the hold capacitor is placed in the negative feedback loop of the amplifier. Thus, the voltage stored across the hold capacitor becomes available at the amplifier output, which is connected to the common output line.
- After the READ phase the circuit is put into the IDLE phase. Switches Hn, An, Cn are open, and Bn is closed. The amplifier is in the voltage follower configuration and the hold capacitor remains floating.

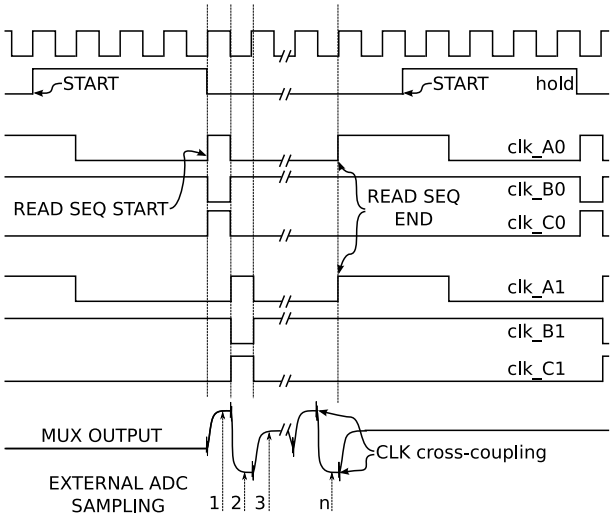

Fig. 6. Timing sequence of a single (in this particular case - first) cell of the shift register. Signal names correspond to switches names in Fig.4.

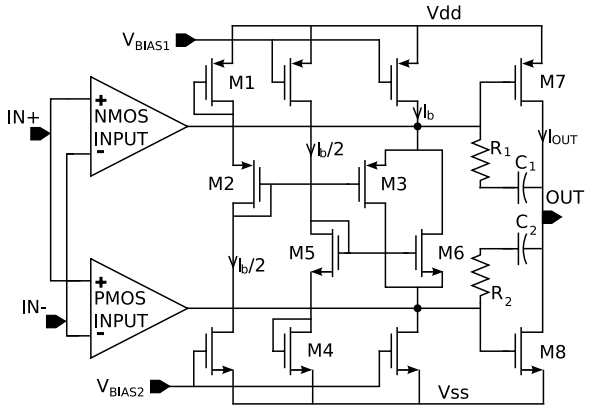

Fig. 7. Schematic diagram of the class AB operational amplifier.

- At the end of the multiplexing sequence the RESET is performed for all the cells simultaneously. Switches Hn and Cn are open while An and Bn are closed. Capacitor C_0 is discharged through switch Bn and the operational amplifier is kept in the voltage follower configuration.

Fig. 6 shows the sequence of signals in one shift register cell. Following the positive edge of the HOLD signal, at first positive CLK edge, signal clk_A0 is set to low and input voltages in all channels are sampled. Negative edge of HOLD_EXT signal triggers the Control Logic Block to initialise the multiplexing sequence.

C. Class AB Operational Amplifier

One of the fundamental requirements for an analogue multiplexer is capability of driving relatively large external capacitive loads. This design issue becomes particularly important in case of a large multiplexing factor, like for example 64:1. The presented multiplexer prototype design comprises only 16 channels, but it is foreseen to be used for multiplexing 64 channels in one ASIC. The parasitic capacitance of the output line plus the capacitances of the S&H output switches Cn (see Fig. 4) can reach up to $4\,pF$ for 64 channels. In order to drive such a capacitance at $5\,MHz$ sampling rate with $\pm 1.3\,V$ output voltage swing an operational amplifier with a large gain-bandwidth product and high slew rate is needed, which can be achieved at expense of high power consumption. On the other hand, low power consumption is a critical requirement for the presented design.

In order to meet these two contradictory requirements an operational amplifier with the class AB output stage has been developed for this project. A simplified schematic diagram of the amplifier is shown in Fig. 7. A rail-to-rail input voltage range is achieved by using two complementary, P-channel and N-channel, differential amplifiers (NMOS INPUT, PMOS INPUT) in parallel [11],[12]. The input amplifiers are single stage, conventional differential amplifiers with active loads, biased with $20\,\mu A$ each. This configuration ensures a rail-to-rail range of the common-mode input voltage. A drawback of this relatively simple solution is variation of the effective transconductance over the full common-mode input range [13]. However, in the foreseen applications we do not expect the common mode signal varying over the full rail-to-rail range. Furthermore, in the S&H circuit the amplifier is used only in the voltage follower configuration so that the effect of varying transconductance is largely reduced by the negative feedback.

The output stage is a class AB amplifier built of transistors M7 and M8, which are driven by first stage amplifiers. Transistors M3 and M6 work as the floating class AB control. Transistor pairs M1, M2 and M4, M5 provide bias voltages to the gates of transistors M3 and M6, respectively. A quiescent current in the output stage is defined by two translinear loops M1, M2, M3, M7 and M4, M5, M6, M8. In the steady state the output current I_{OUT} is defined by dimensions of the matched transistor pairs M1, M7 and M4, M8 according to (1) [13].

$$I_{OUT} = I_b \frac{(W/L)_7}{(W/L)_1} = I_b \frac{(W/L)_8}{(W/L)_4} \tag{1}$$

Dimensions of the floating current mirror transistors M2 and M3 are equal and set to $W/L = 4\,\mu m/0.4\,\mu m$, dimensions of M5 and M6 are set to $W/L = 2.5\,\mu m/0.5\,\mu m$.

The frequency response of the amplifier is compensated by capacitors C_1 and C_2 using the classical Miller technique and serial resistors R_1 and R_2. The slew rate of the amplifier depends mostly on the bias current of the input stage and the load capacitance. For a bias current of $20\,\mu A$ in the input amplifiers and load capacitance of $4\,pF$ we obtain a slew rate of $25\,V/\mu s$ at quite low total power of $0.28\,mW$ for the power supply voltage of $3.3\,V$. This slew rate is perfectly sufficient for a multiplexing period of $200\,ns$ and signal swing $\pm 1.3\,V$.

D. Output Buffer

The same amplifier architecture as in the S&H circuit has been employed in the output buffer. The requirements for the output buffer depend primarily on the external load capacitance to be driven. For the presented design we have assumed that the buffer should be able to drive a load capacitance

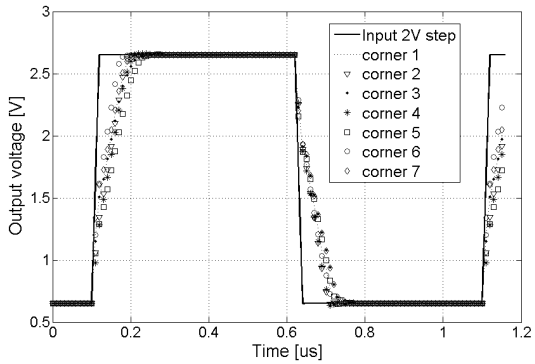

Fig. 8. Transient simulation of the operational amplifier for various sets of corner parameters.

up to 12 pF without degrading settling time of the output signal compared to that obtained at the multiplexer output. Thus, the slew rate of the output buffer should be at least $25\,V/\mu s$ for a load capacitance of 12 pF. This has been achieved for dimensions of the output transistors M7 and M8 set to $W/L = 800\,\mu m/0.6\,\mu m$ and $W/L = 400\,\mu m/0.6\,\mu m$ respectively. The resulting power consumption of the buffer is $1.3\,mW$, which is fully acceptable given that there will be only one such buffer per 64-channel ASIC.

E. Immunity of Process Variation

A particular design effort has been made to minimise the influence of process variation on the circuit parameters, though some sensitivity of the circuit parameters to process variation is unavoidable. Figure 8 shows the simulated transient responses of the operational amplifier working in the follower configuration, loaded with $5\,pF$ capacitance, for seven sets of corner parameters recommended by the technology vendor. A phase margin of 70° ensures that the step response does not show any ringing. Obviously the slew rate of the amplifier and so the settling time depends on the process parameters but the latter does not exceeds $150\,ns$ for the worst case corner parameters.

F. Multiplexer Layout

Single cell of the multiplexer occupies an area of $80 \times 186\,\mu m^2$. The mask layout is presented in Fig. 9. The width of the cell was set to $80\,\mu m$ to match to the pitch of the amplifier/filter channel. Particular effort has been made to shield the output line in order to minimise pick-up of the switching noise.

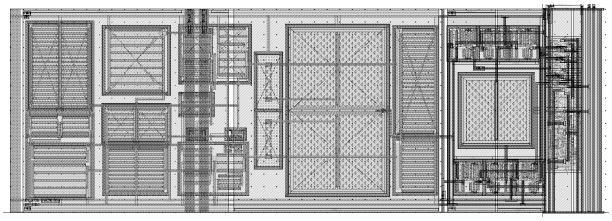

Fig. 9. Layout of a single multiplexer cell.

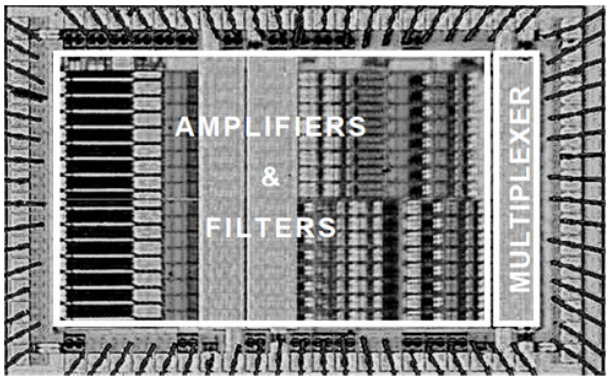

Fig. 10. Microphotograph of the prototype chip.

III. Test Results

The presented 16-channel multiplexer has been fabricated as a part of the prototype chip comprising also 16 channels of preamplifier and filter circuits. The chip has been fabricated in an N-well, 4-metal, 2-poly, $0.35\mu m$ CMOS process. A microphotograph of the prototype chip is shown in Fig. 10.

Since the multiplexer is integrated with the amplifier/filter channels the input signals to the multiplexer can be delivered only through the amplifier and filter circuits. Therefore basic tests have been performed for the sine wave signals. Digital control signals were generated using an FPGA board. The generator module implemented in the FPGA allows adjustment of clock period, sampling rate, sampling time and multiplexing rate to test various multiplexer parameters. Figure 11 illustrates the functionality of the multiplexer. It shows six $1\,kHz$ sine wave signals of different amplitudes sampled and multiplexed to single output. Input amplitudes were swept from $175\,mV$ to $1050\ mV$, sampling rate was $50\ kHz$ and multiplexing frequency $5\,MHz$.

Figure 12 shows single-shot responses at the multiplexer output recorded for input signal of $1.3\,V$, positive and negative respectively. The signals have been recorded in a digital oscilloscope via the passive probe $10/1\,M\Omega - 16\,pF$, which was driven directly by the buffer amplifier integrated in the multiplexer. The settling time for signal $\pm 1.3\,V$ is $70\,ns$,

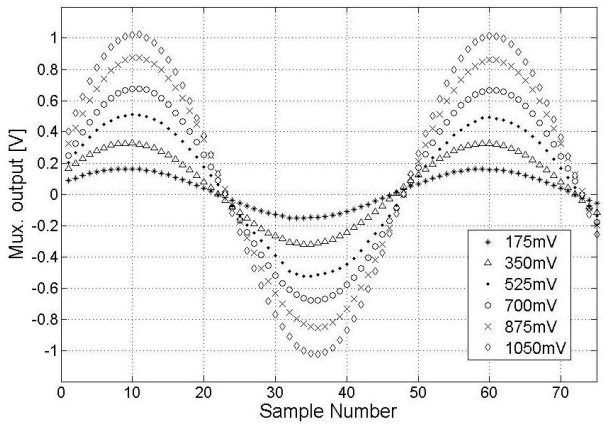

Fig. 11. Sampled sine waveforms - amplitudes swept from 175 mV to 1050 mV, sampling rate 50 kHz, clock frequency 5 MHz.

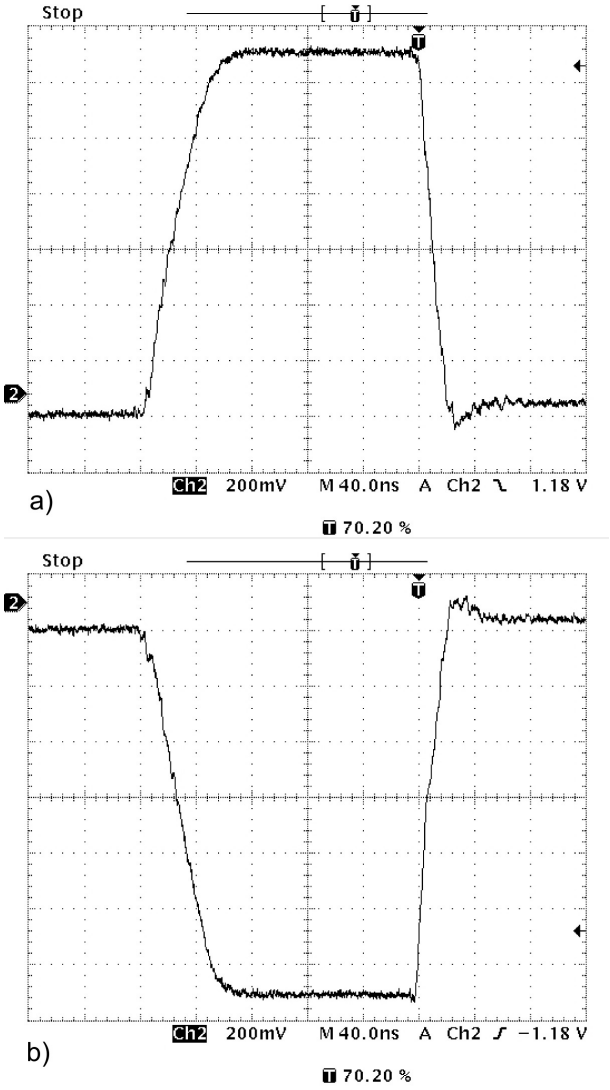

Fig. 12. Multiplexer response for positive (a) and negative (b) input signal of $1.3\,V$.

which is sufficient for operation of the multiplexer at $5\,MHz$ multiplexing rate.

IV. Summary

We have developed a low power, high dynamic range S&H circuit and analogue multiplexer to be used as a building block in multi-channel ASICs for recording neural signals from alive neural tissue. The circuit has been designed in a $0.35\mu m$ CMOS process for power supply voltages $\pm 1.65\,V$. The S&H circuit is based on a switched capacitor technique, which allows us to reduce sensitivity of the circuit to power supply noise. A dedicated low power class AB operational amplifier has been developed for the S&H circuit. A novel shift register implemented in the walking one schema allows us avoiding clock feed-through glitches in the middle of the multiplexing periods, which are common problem in conventional designs using standard D-latch shift registers. The prototype circuit comprising sixteen cells has been manufactured and tested as a part of 16-channel ASIC comprising also prototype amplifier and filter circuits. An output buffer, which can drive external load capacitance up to $12\,pF$ has been integrated in the chip. The test results show good agreement with the simulations and proof that the required performance has been achieved. Basic parameters of the circuit are summarised in Table I.

TABLE I
Summary of Basic Electrical Parameters of the Analogue Multiplexer

Power supply voltages	$\pm 1.65\,V$
Power dissipation per channel	$0.28\,mW$
Maximum sampling rate	$70\,kHz$
Maximum multiplexing rate	$5.12\,MHz$
Minimum sampling time	$600\,ns$
Maximum input/output dynamic range	$\pm 1.3\,V$
Sample and hold Op-Amp slew rate	$25\,V/\mu s$
1.3 V step settling time	$70\,ns$

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