

A 800 μ W 1GHz Charge Pump Based Phase-Locked Loop in Submicron CMOS Process

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Abstract—Demand of modern measurement systems in sub-micron CMOS process introduced new challenges in design of low power high frequency clock generation systems. Technical possibilities for clock generation using classical oscillator based on a quartz filter is limited to tens of megahertz. Thus, 1 GHz clock generation is not possible without a frequency multiplier system. It is difficult to achieve, because in submicron process, where the integration of analog and digital blocks poses serious challenges. The proposed solution is a low power charge pump phase-locked loop (CPPLL) with the center frequency of 1 GHz. It combines various modern circuit techniques, whose main aim is to lower power consumption, which is below 800 μ W for the whole PLL, while maintaining good noise properties, where the jitter rms is 8.87 ps. The proposed phase-locked loop is designed in 0.18 μ m CMOS process.

Keywords—Charge pump phase-locked loop, CPPLL, phase-locked loop, PLL, frequency multiplication, VCO, CCO, charge pump, PFD, V-I converter.

I. INTRODUCTION

ALTHOUGH the basis of the phase-locked loop remained unchanged since its invention, its implementation in various technologies and for different purposes does not cease to be a challenge for its designers. Phase-locked loop is a closed loop system with a feedback, which aims to establish a permanent relationship between phase of the input and the output signal. Nowadays, consumer electronics application areas of PLL are very wide. They work in all devices where a clock generation unit (CGU) is required, however their architecture depends on application.

For this work the most important point is the frequency multiplication. In applications requiring a high frequency CGU, the technical possibilities for clock generation using the classical oscillator based on a quartz filter is limited to tens of megahertz. These limitations are increased by the technology of printed circuits boards, whose parameters are not sufficient to generate and transfer 1 GHz signal to the chip. This problem can be fully resolved by the PLL.

Recent years have seen a strong growth of interest in phase-locked loops, because it is the most effective way of frequency multiplication. There are many modifications of classical solutions: there are analog ([1]), purely digital ([2]) and mixed designs ([3], [4], [5], [6], [7], [8]). Especially the latter guarantees obtaining the most beneficial outcomes relevant to this study, by combining good noise properties of analog blocks and low power consumption of digital blocks. There are many parameters characterizing the phase loops,

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both individual functional blocks and the whole system. Many of them are specific to the particular architecture and the application of the module. For this design the main parameters are current consumption, size of the module, and good noise performance.

This paper is organized as follows: Section II describes phase-locked loop architecture including PLL block diagram, power consumption and noise considerations. In Section III PLL design at circuit level is presented with all blocks in detail. The performance of all circuits is verified in Section IV with simulation results and additional means to compensate and improve some properties. Summary and closing remarks are in Section V.

II. SYSTEM OVERVIEW

A. Architecture

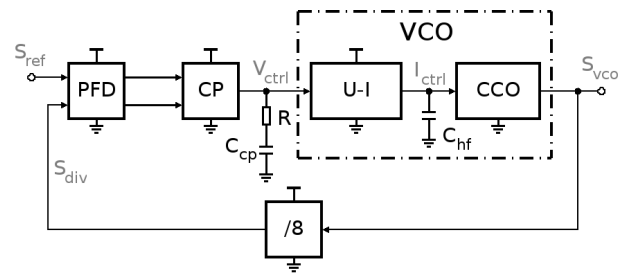


Fig. 1. Charge pump phase locked loop block diagram.

The chosen architecture is the charge pump phase-locked loop with frequency divider that uses a fixed, non-programmable value. The block diagram of the PLL is shown in Fig. 1. It consists of a phase-frequency detector block (PFD) which cooperates with a charge pump (CP) and produces a square wave with duty cycle proportional to the phase error between the reference input (S_{REF}) and the feedback output (S_{DIV}). This signal is converted to DC value by a second order loop filter, which consists of the capacitor C_{CP} , the resistor R and high frequency pole created by C_{HF} . The voltage V_{CTRL} is converted to current I_{CTRL} by the next block and current controlled oscillator (CCO) generates desired 1 GHz output signal. Part of the output signal is fed back to the PFD through the frequency divider, whose division ratio is set to eight.

B. Power and Area Reduction

The key point in this design is the use of a ring oscillator type VCO combined from CCO and voltage-to-current converter. Ring oscillator is considered to be noisy but has a huge advantage over cross coupled LC VCO its power consumption

and design area are negligible. To reduce power consumption even more this design uses a frequency divider and PFD in the TSPC (True Single Phase Clock) logic.

C. Noise Reduction

The CPPLL architecture is characterized by good noise properties, especially suppressing high frequency noise caused by the oscillator. This is achieved by a high frequency filter, that suppresses well noise from the oscillator, but not good enough in-phase noise (noise from reference oscillator, PFD and CP). But because this work uses a high stability reference circuit based on a quartz filter at the frequency of 125 MHz, the problem with low frequency noise is resolved. Additionally to reduce more in-phase noise this design uses differential charge pump with additional dead zone pulses reduction circuit. By use of pseudo-differential CCO and differential CP this design also highly reduces power line noise coupling.

III. PHASE-LOCKED LOOP DESIGN

A. Current Controlled Oscillator

VCO is the main and the most important block of the entire loop. Spectral purity of output signal and fulfilling the demands of the target system will depend on it. Optimization of its properties is imposed by the requirements for the entire loop, in which the focus is on minimization of power consumption. The block diagram (Fig. 1) shows that the VCO consists of two parts: voltage-to-current converter and CCO separated by a capacitor (C_{HF}), which introduces a second pole to the loop filter transmittance.

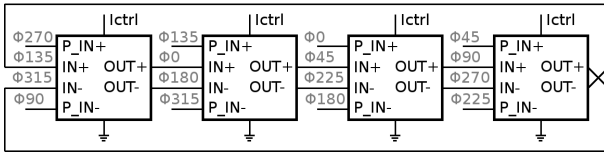


Fig. 2. Pseudo-differential current controlled oscillator.

As a CCO, pseudo-differential quadrature generator is used, adopted from [7], and its schematic is shown in Fig. 2. Its differential structure and current control makes it less susceptible to the noise from the power supply, which is essential in mixed-signal integrated circuits.

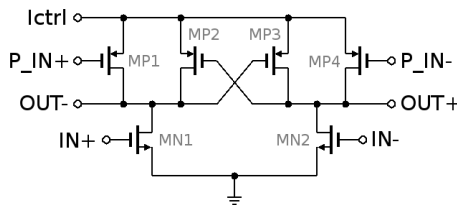


Fig. 3. CVSL inverter as a CCO delay stage.

Delaying element is shown in Fig. 3. It is a differential inverter in the CVSL (Cascode Voltage Switch Logic) logic enriched with a pair of transistors (MP1, MP4), which reduces the slew rate. The delay of the stage is inversely proportional to

the current I_{CTRL} and the output frequency is also inversely proportional to the delay, so the gain of the CCO, K_{CCO} should be constant in wide range of frequencies. Sizes of used transistors have been matched to achieve CCO center frequency at 1 GHz.

Differential to single-ended conversion is shown in Fig. 4. It is based on a simple differential converter (Fig. 5) constructed from differential pair (transistors MN1 and MN2) with a cross coupled load (transistors MP1 and MP2). This treatment introduces a positive feedback, which increases the gain of the stage.

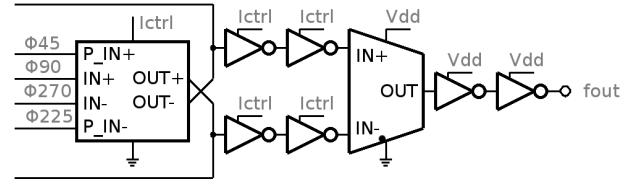


Fig. 4. CCO differential to single ended conversion.

In addition, buffers are placed before the converter, which aim at improving the slew rate without duty cycle distortion. Objective is achieved through using of current starved buffers rather than supplying them with VDD line.

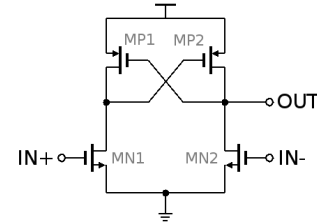


Fig. 5. Differential to single ended converter.

B. Voltage-to-Current Converter

The block that provides the necessary controlling current for CCO is the voltage-to-current converter shown in Fig. 6. Its task is to buffer capacitance of the filter against discharge, improve linearity of CCO tuning curve and make the gain of CCO independent of currently generated frequency. It also reduces the impact of voltage ripple (V_{CTRL}), which directly changes the output frequency.

Obtaining the desired linearity of the tuning curve is impossible in the classical common source stage configuration due to quadratic dependence of drain current I_D with the changes of the gate voltage V_{GS} . Therefore, transistor MN1 is in the common source stage with source degeneration configuration, which is provided by resistor R2. It causes a part of the input voltage change to appear across it, rather than as overdrive voltage of the transistor MN1 [9]. Then the current through PMOS and NMOS current mirrors (MP1, MP2 and MN2, MN3 respectively) flows into a regulated drain cascode current mirror [10]. Real current mirror has a finite output resistance, which could be significantly increased using just regulated drain cascode current mirror, which maintains the drain of the transistor MN8 at a fixed potential. Cascode mirror is

built of MP3, MP4, MP7 and MP8 transistors, while the drain regulating amplifier is composed of a differential pair MP5, MP6 and the MN4 and MN5 load biased by NMOS current mirror (MN2, MN3).

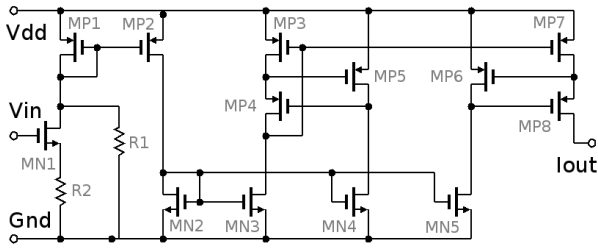


Fig. 6. Voltage to current converter.

C. Phase-Frequency Detector

The proposed solution is shown in Fig. 7. It is a phase-frequency detector with a short duration of the reset path adopted from [11]. PFD operation is the same as in a standard detector [12], but implementation is close to dynamic flip-flop in TSPC logic. The resetting module has been implemented differently in relation to the conventional method. When both signals (up and down) are in the high state then the reset is started, but the slave part has an asynchronous reset and the master part is resetting synchronously. PFD is completely symmetrical, there is no division in its construction between the master and the slave block, the master block is chosen when first upcoming signal appears.

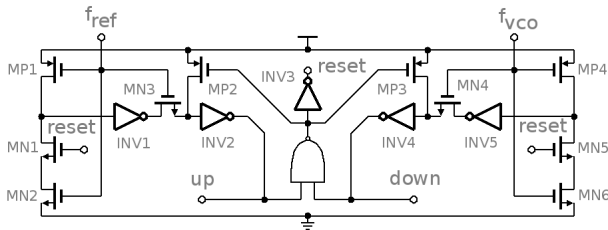


Fig. 7. Phase-frequency detector.

Synchronous reset in PFD increases the maximum operating frequency and significantly reduces power consumption. In [11] a slight increase of the maximum frequency was achieved, but for the project presented in this paper it is not so important because of the relatively low frequency for PFD (125 MHz). This design also reduced by half the power consumption compared to conventional PFD, which was a reason to use concepts from this circuit.

D. Charge Pump

Designing the charge pump started with the simplest model [12], PMOS and NMOS current sources with two simple switches controlled by up and down PFD signals. With it, PLL operates correctly assuming that PMOS and NMOS

current source give the same currents. Nevertheless, the basic configuration of PMOS and NMOS current source is far from ideal and the difference between the current causes the static phase error and unevenness of the charge pump gain. Another problem occurs if both switches are off, PMOS current source sets the switch terminal to the positive voltage and NMOS current source sets second switch to ground. Every switch introduces parasitic capacitance, so when both switches turn on, a voltage jump occurs on the common node V_{CTRL} to compensate voltage difference. This introduces a periodic voltage disturbance and additional harmonics in spectrum of the generated signal [12].

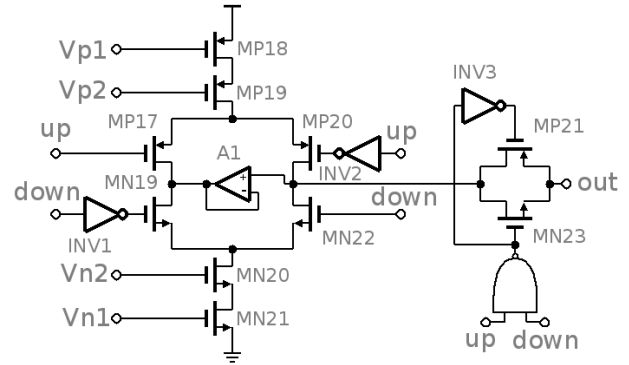


Fig. 8. Differential charge pump.

Solution for the posed problems is the charge pump presented in this paper shown in Fig. 8. It consists of two current sources (NMOS and PMOS) and four switches. The loop filter is connected to the output of the transmission gate, which in addition is switching the charge pump output current. Comparing to the standard configuration, this solution introduces two additional switches, which are toggled with inverted signals by inverters INV1 and INV2. This has provided a dual current flow path, during high state on up and down signals the current flows through transistors MP20 and MN22 but when both signals are in the low state, the current flows trough MP17 and MN19 transistors. To eliminate the impact of parasitic switches capacitance, it is necessary to use an amplifier A1, which sets nodes between switches to equal potential. The schematic of used amplifier is shown in Fig. 9, it works in voltage follower configuration. The amplifier is built from differential pair (MN1, MN4) with a current mirror load (MP1, MP2) and the tail current source biased by the charge pump biasing circuit.

The described charge pump requires a biasing system, which aims to tackle the second defect of the simplest configuration the mismatch of PMOS and NMOS current sources. Biasing circuit is based on constant gm current reference, sometimes called beta multiplier, which is shown in Fig. 10 [10]. Circuit consists of two current mirrors, PMOS (MP2, MP5) and NMOS (MN3, MN6), which mirror each other's current. Due to the created positive feedback it is necessary to reduce it by the introduction of resistor R1, which cuts the feedback and creates itself as a current reference.

Transistor size minimization in current mirrors is possible through the introduction of an amplifier, which holds potentials

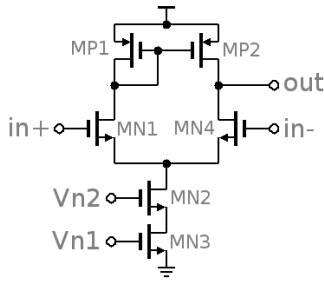


Fig. 9. Charge pump differential amplifier.

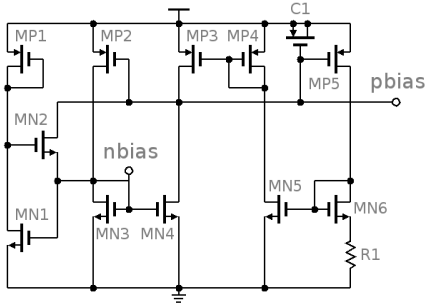


Fig. 10. Current reference - constant g_m circuit.

between mirrors at the same level, in similar manner as it was proposed in the voltage-to-current converter (Fig. 6). The amplifier is created from the differential pair with PMOS mirror load, without typically used NMOS current sink. The current sink in this solution is unnecessary because the input signal is coming directly from the current mirror base node and that keeps differential pair working in saturation range.

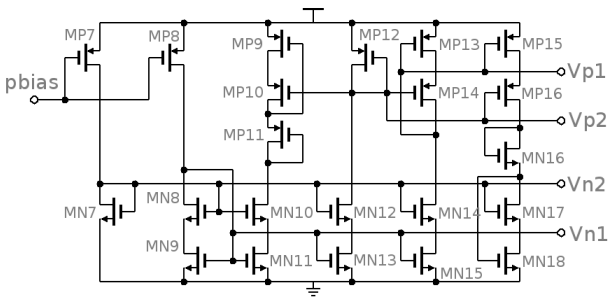


Fig. 11. Charge pump biasing circuit.

This reference needs a startup circuit built from transistors MN1, MN2, MP1, which after setting the required operating point does not dissipate current and does not disturb the reference. Additionally, for stability reasons 0.8 pF capacitor is placed (C1), built on zero threshold voltage transistor. The output from the constant gm circuit goes to the cascode biasing circuit [10] shown in Fig. 11, whose aim is to bias the current sources of the charge pump, so that the currents do not depend on power supply and the loop filter voltage ripple (V_{CTRL}).

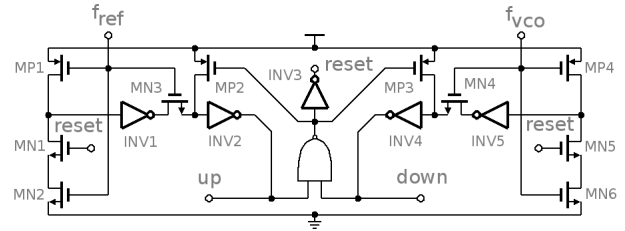


Fig. 12. Frequency divider in TSPC logic.

E. Frequency Divider

The frequency divider consists of three D-type flip flops in modulo 2 configuration in TSPC logic adopted from [13]. A single stage, divided by 2 circuits, is shown in Fig. 12. In relation to the solution presented in the publication [13] inverter is added to the output to improve the slew rate (transistors MP5, MN6).

IV. RESULTS

A. Results of Particular Blocks

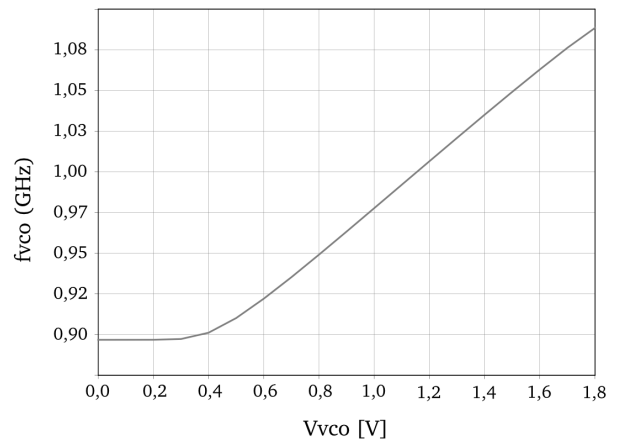


Fig. 13. VCO tuning curve.

The voltage controlled oscillator tuning curve (CCO with voltage-to-current converter) is shown in Fig. 13. In addition to obtained linearity, the gain reduction can also be observed. It is done by resistor R1 (Fig. 6), which significantly reduces the noise, since the output frequency is not as sensitive to small variations of the loop filter voltage V_{CTRL} .

Phase noise of the VCO is shown in Fig. 14, while jitter cycle J_C and jitter cycle-to-cycle J_{CC} are in Tab. I for rms and peak-to-peak values. The phase noise characterization was carried out from 10 Hz to 500 MHz from center frequency (1 GHz). The noise of the ring oscillator type VCO is dominated by low frequency noise. It can be seen on the chart as a 30 dB/dec slope, which at the end of the graph ceases to be dominant to the white noise, 20 dB/dec. The jitter was calculated from the phase noise based on the relationship set out in the publication [14] in the range of frequencies from 10 Hz to 500 MHz.

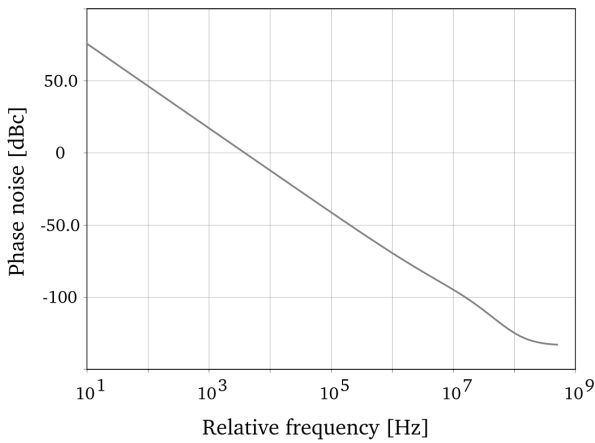


Fig. 14. VCO phase noise.

Fig. 15 shows the corner analysis results, where corner parameters (cor1-cor8) are set according to the process recommendations to take into account the scattering of all process parameters, temperature and supply voltage. The dispersion of the VCO center frequency was shown, while control voltage was set to the value that fits the center frequency of typical parameters corner cor1 to 1 GHz.

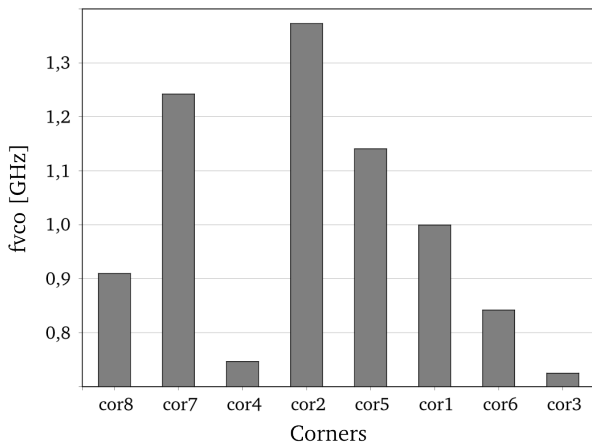


Fig. 15. VCO corner analysis.

The figure shows a considerable scattering of the generated frequency from 650 MHz to 1.5 GHz, but this is not surprising. Generated frequency depends on the delay of the single stage and since the delay is changed for the case of faster or slower working transistors, it must also change the generated frequency.

TABLE I
VCO JITTER

Jitter	rms [ps]	p-p [ps]
J_C	1.25	7.75
J_{CC}	1.51	9.33

Tab. II presents the results of power consumption comparison between both implemented phase-frequency detectors. The

first from publication [12] and the second used in this work (adopted from [11]).

TABLE II
PFD POWER CONSUMPTION COMPARISON

PFD type	Power [μ W]
DFP	21
TSPC-like	17

By applying the circuit from [11] a 50% power reduction was not reached (as presented in that paper), but the power was reduced significantly. Possible reason for this is relatively low PFD input frequency and use of a modern technology comparing to that used in the original solution.

Mismatch between PMOS and NMOS current sources is shown in Fig. 16. The obtained result provides 10% current stability in the 1 V range of the loop filter voltage tuning. It is therefore essential to set 1 GHz output frequency in the middle of loop filter voltage range. To eliminate the influence of the mismatch of the currents at the loop filter voltage extreme values an additional circuit is added. Namely, the output of the charge pump is preceded by a symmetric switch, which shortens the time when both current sources are on and introduce larger mismatch.

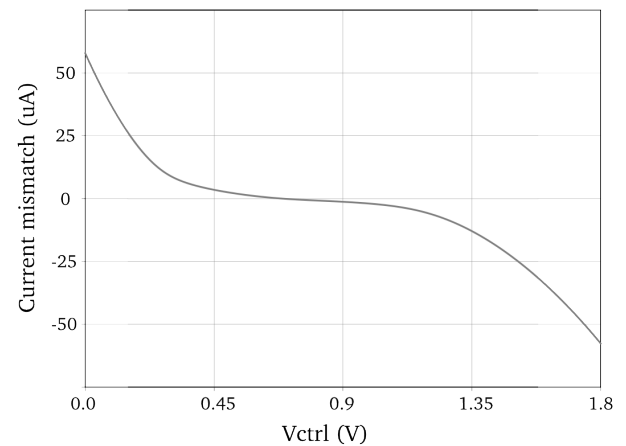


Fig. 16. Charge pump current mismatch.

By applying minimum sized transistors, which are provided by the technology ($W=240$ nm, $L=180$ nm) transmission gate degrading effect is negligible compared to achieved results. The time plot during particular situation showing current mismatch reduction for the loop filter voltage $V_{CTRL}=1.6$ V is shown in Fig. 17.

Tab. III presents the comparison of the frequency divider with TSPC logic and D-type master-slave frequency divider. Power consumption of TSPC frequency divider is almost two times lower and the jitter is also significantly reduced.

TABLE III
FREQUENCY DIVIDER COMPARISON

Divider type	Power [μ W]	J_C rms [ps]
DFP-MS	70	0.52
TSPC	45	0.36

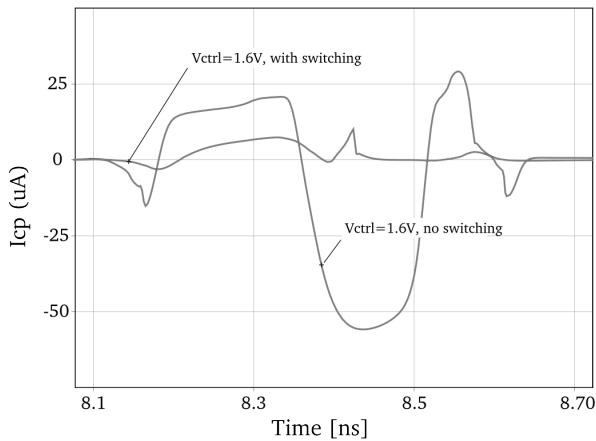


Fig. 17. Charge pump current mismatch reduction.

B. Corner Analysis Correction Circuit

Many solutions using ring oscillators are facing similar problem in the corner analysis. Often used solution is to use a wider tuning curve for use of greater range of frequencies, which increases the gain K_{VCO} . However, the gain increase causes that the output frequency is more sensitive to the control voltage, which in broadband phase loops increases noise significantly. The solution proposed in this paper is to digitally change value of resistor R1 in the voltage-to-current converter (Fig. 6). This resistor is responsible for VCO gain limitation and by changing its value it is possible to set appropriate frequency range. The scheme and resistance values are shown in Fig. 18. They have been matched to the worst cases in the corner analysis (Fig. 15). The resistance tuning uses serial switching because it significantly reduces the size and the area in relation to parallel switching.

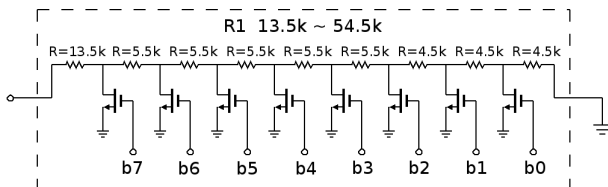


Fig. 18. VCO center frequency variations correction circuit.

C. Summary of Results

TABLE IV
COMPARISON WITH EXISTING SOLUTIONS

Reference	[5]	[4]	[8]	[9]	[10]	[2]	This
Tech. [nm]	90	180	130	180	350	250	180
Vdd [V]	1.0	1.8	1.2	1.8	3.3	2.5	1.8
From [GHz]	0.5	0.8	1.0	0.5	0.0	0.1	0.9
To [GHz]	2.0	3.0	3.0	2.5	1.9	1.6	1.1
J_C [ps]	5.8	3.7	0.4	2.4	5.7	3.3	8.9
$J_C(n)$ [ps]	5.8	5.6	1.0	5.7	4.6	3.3	8.9
Power [mW]	0.7	3.3	23	25	20	10	0.8
Power(n) [mW]	4.5	2.2	29	10	3.8	3.7	0.8

Tab. IV presents a comparison of parameters obtained in this work to other publications. The presented publications

differ in process, supply voltage value and frequency, which affect the jitter and power consumption. Hence parameters for comparison purposes were normalized according to the scaling equations [15] to the parameters of this work - 180 nm process, 1.8 V supply voltage and 1 GHz output frequency. Normalized values are indicated as (n) in Tab. IV. Solution presented in this paper shows the lowest power consumption, which was the aim of this work. This is done at the expense of frequency range and jitter, which are still at a satisfactory level.

V. CONCLUSION

The article presents the problem of frequency multiplier and describes a design of a low power charge pump phase locked loop for 1 GHz frequency. Circuits schematics and description were presented including simulation parameters necessary for proper system operation. Achieved power consumption is less than 800 μ W while maintaining good noise properties, while the jitter is at the level of 8.87 ps.

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